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# Auto Zero Negative Feedback and Current Distributed Load to Decrease Offset of Buffer Amplifier

***Ranjana Kumari Mishra* and Teena Raikwar*****

**M. Tech scholar, NIIST Bhopal, (MP), INDIA*

***Assistant Professor, NIIST Bhopal, (MP), INDIA*

*(Corresponding author: Ranjana Kumari Mishra)*

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**ABSTRACT: In this paper an auto zero negative feedback and current distributed load is discussed. Current distributed load is used to increase the DC gain of operational amplifier and negative feedback auto zero is used to cancel the offset by sampling phase and output phase. The circuit is simulated in Microwind 3.1 layout tool.**

## I. INTRODUCTION

Liquid crystal display panel is now used in every portable display devices and they are generally battery operated. The requirement of high resolution display is the increasing demand for today's world. To increase the resolution of display panel the resolution of digital to analog converter should be high means it will divide the reference voltage to as small as possible suppose there is 10bit DAC then it resolution for a reference voltage is $V_{ref}/2^n$ where n is equal to 10. To drive a pixel information, we need driver circuit in LCD panel there is two driver circuit one is source driver circuit and another is row driver circuit. The work of source driver is to display the required information on pixel and the work of gate driver is to refresh the pixel with required refreshing rate. The source driver consist of shift register, input register, data latches, level shifter, digital to analog converter, pre-emphasis and analog output buffer as shown in fig 1.The speed to drive a pixel is depend upon the speed operation of analog buffer .For high resolution one condition must be fulfill by buffer and DAC both as the offset of buffer should be less than the resolution of DAC if it is not possible than the information will be lost. Lu et al. [5]–[10] proposed some class-AB output buffers for flat-panel-exhibit application, for which the driving capabilities of the circuit are achieved by integrating comparators which sense the elevating and/or falling edges of the input waveform to turn on a push/pull transistor to charge/discharge the output load. Yu *et al.* proposed a class-B output buffer for flat-panel-exhibit column driver, for which a comparator was utilized in the negative feedback path to eliminate the quiescent current in the output stage. Kim *et al.* [6] proposed a multi-level multi-phase charge-recycling method for low-power AMLCD column drivers.

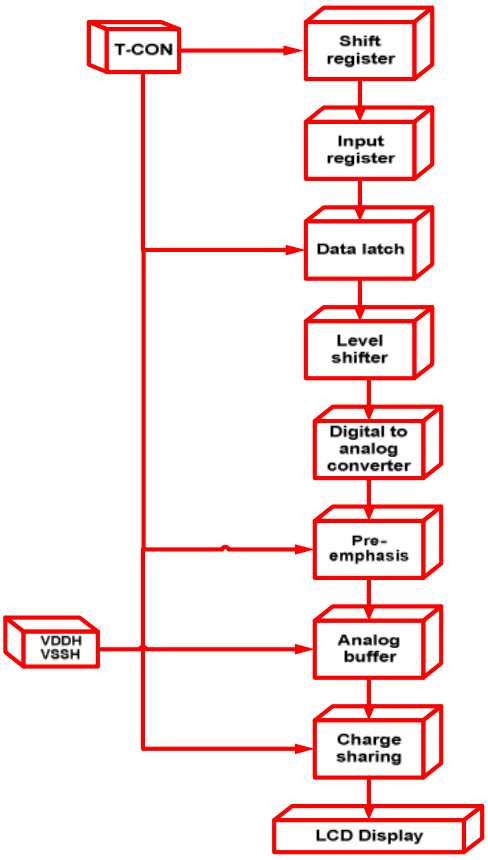


**Fig. 1.** LCD source driver architecture.

The author proposed this charge-recycling method to reduce the potency consumption incurred in driving highly capacitive column lines by storing the charge into the external capacitors and reusing it in the next cycle.

Itakura *et al.* proposed an output amplifier in which the phase emolument is achieved by introducing a zero, which is composed by the load capacitance and the phase emolument resistor connected between the output of the amplifier and the capacitive load.

To achieve high resolution for LCD panel DAC resolution should be high and the offset of buffer should be less than resolution of DAC. So, two rudimentary offset abrogation structures with their simple structure are commonly utilized in LCD source driver, which are chopper and auto-zero.

Fig. 2 shows the structure of auto-zero which is used to remove the offset . The rudimental concept of auto-zero is sampling. It samples the offset voltage and stores in a capacitor in sample state. In output state it abrogates the offset voltage due to law of charge conservation. It utilizes three switches and one capacitor to achieve auto-zero. Customarily in LCD source driver uses metal-in-metal (MIM) capacitor as storage capacitor that it won't increase the area of source driver.

The simple structure of auto-zero is additionally utilized in some prior researches for offset abrogation [8].

By Chih-Wen Lu and Chung Len Lee "A Low-Power High-Speed Class-AB Buffer Amplifier for Flat-Panel-Display Application"-A low-power, high-speed, but with a large input dynamic range and output swing class-AB output buffer circuit, which is suitable for the flat-panel display application, is proposed. The circuit employs an elegant comparator to sense the transients of the input to turn on charging/discharging transistors, thus draws little current during static, but an improved driving capability during transients. It is demonstrated in a 0.6 m CMOS technology [11].

With the evolution of compact, light-weighted, low-power, and high quality display, there is a big demand of developing the low-power consuming, high efficiency, and high-speed buffer circuit. The circuit should occupy a small die area, consume minimal power, have a settling time smaller than the horizontal scanning time, and a capability of offering high-current resolution which can accommodate up to 256gray levels. For a 4 V of full scale, each gray level corresponds to 16mV [1], [2]. Some output buffers were proposed and demonstrated in recent years. For examples, Yu *et al.* [3] proposed a class-B output buffer for flat-panel-display column driver, for which a comparator was used in the negative feedback path to eliminate the quiescent current in the output stage; Lee *et al.* [4] proposed a dynamic-bias technique, to increase the bias current of the differential input stage of a two-stage amplifier when the input voltage difference is large; and Khorramabadi [5] also proposed a class-B amplifier which had a better power efficiency but with a large-output transistor.

In this work, a class-AB CMOS output buffer circuit is proposed. The circuit achieves the large driving capability by employing a simple but elegant comparator circuit to sense the transients of the input to turn on charging/discharging transistors, which are statically "off" when no input is applied. This increases the speed of the circuit without increasing too much static-power consumption. The circuit also features a wide input voltage range and a large output swing.

Fig. 2 shows the proposed class-AB buffer circuit. As a buffer, the output is connected to the inverting input (in) and the input signal is applied to the non-inverting terminal (in+). The differential pair M5–M6, which is biased by the constant current source M1–M4, is actively loaded by the current mirror formed by M7 and M8. M9 andM10 form a common-source output stage and the Miller-feedback R-C is for frequency compensation.

By Chih-Wen Lu, Member, IEEE High-Speed Driving Scheme and Compact High-Speed Low-Power Rail-to-Rail Class-B Buffer Amplifier for LCD Applications-A high-speed driving scheme and a compact high-speed low-power rail-to-rail class-B buffer amplifier, which are suitable for small- and large-size liquid crystal display applications, are proposed. The driving scheme incorporates two output driving stages in which the output of the first output driving stage is connected to the inverting input and that of the second driving stage is connected to the capacitive load. A compensation resistor is connected between the two output stages for stability. The second output stage is used to improve the slew rate and the settling time. The buffer draws little current while static but has a large driving capability while transient. The circuit achieves the large driving capability by employing simple comparators to sense the transients of the input to turn on the output stages, which are statically off in the stable state. This increases the speed of the circuit without increasing static power consumption too much. A rail-to-rail folded-cascade differential amplifier is used to amplify the input signal difference and supply the bias voltages for the second stage. The output buffers, which are usually made of operational amplifiers, are used to drive highly capacitive column lines of the display panel. Because the load capacitance depends on the size of the display panel, the output buffer should drive a wide range of load capacitance. In addition, because the buffer amplifiers are required to have a high open-loop gain to obtain a low value of the systematic offset voltage, a two-stage buffer amplifier is usually used in the LCD driver,. This two-stage amplifier requires compensation for stability and the conventional compensation scheme requires a Miller capacitance, which occupies a large area in an LCD driver.

Some buffer amplifiers adopt the output node as a dominant pole to achieve enough stability without a Miller capacitance. For example, Lu*et al.* [9] proposed a class-AB output buffer for flat panel display application, where the driving capability of the circuits achieved by adding comparators which sense the rising and/or falling edges of the input waveform to turn on a push/pull transistor to charge/discharge the output load.

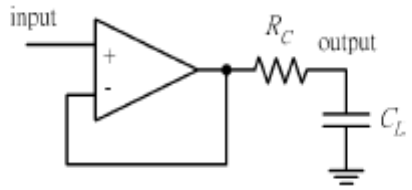


**Fig. 2.** Configuration of the buffer amplifier with the zero compensation.

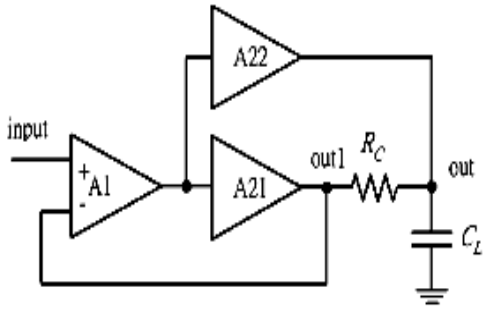


**Fig. 3.** Configuration of the proposed driving scheme.

A rail-to-rail amplifier with an offset cancellation, which is suitable for high color depth and high-resolution liquid crystal display (LCD) drivers, is proposed. The amplifier incorporates dual complementary differential pairs, which are classified as main and auxiliary transconductance amplifiers, to obtain a full input voltage swing and an offset canceling capability. Both offset voltage and injection-induced error, due to the device mismatch and charge injection, respectively, are greatly reduced. The offset cancellation and charge conservation, which is used to reduce the dynamic power consumption, are operated during the same time slot so that the driving period does not need to increase. An experimental prototype amplifier is implemented with 0.35- m CMOS technology. The circuit draws 7.5 A static current and exhibits the settling time of 3 s, for a voltage swing of 5 V under a 3.4 k resistance, and a 140 pF capacitance load with a power supply of 5 V. The offset voltage of the amplifier with offset cancellation is 0.48 Mv.

This paper presents a design and implementation of an output buffer for LCD Driver with rail-to-rail voltage swing using TSMC 0.35 pm 2P4M process at 5V supply.

We designed a class-B output buffer with offset compensation ability to reduce the nonlinearity of output voltage. It performs a rail-to-rail swing range and high slew rate of 14 V / us and 11.5 V / us for rising and falling edges under a 400 pF capacitance load. For high driving capability, two push-pull output stages are used, two frequency compensation stages are also introduced for stability, One is the miller compensation with 0.04 pF capacitance , and the other is zero compensation with 0.1 kΩ added between two push-pull output stages for stable driving under different capacitance loads. The result exhibits the settling times of 0.7 gs for rising and 0.85 ps for falling edges with voltage swing 5V under a 400 pF capacitance load. Even under a 1000 pF capacitance load, it still has the settling time of 1.52 us and 1.80 us for rising and falling edges , respectively. The effective area of this buffer is only 100 x 100 pm' with build-in offset voltage holding capacitor (Guo-Teng *et al.*, 2009). C.H. Tsai J.H. Wang H.Y. Zheng C.T. Chang C.Y. Wang "A new compact low-offset push–pull output buffer with current positive feedback for a 10-bit LCD source driver" Published in IET Circuits, Devices & Systems Received on 4th January 2010. In this study, a low-offset push–pull output buffer and an area-efficient resistor-capacitor digital-to analogue converter for a 10-bit liquid crystal display (LCD) source driver are presented. Compared to other push-pull output buffers, the proposed output buffer has a smaller area and lower power consumption.

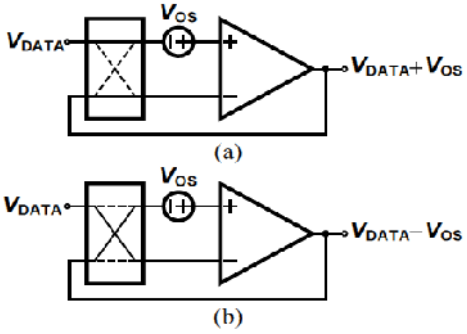


**Fig. 4.** Chopper output (a) positive offset voltage (b) negative offset voltage.

Two complementary push–pull output buffers driving a pair of column lines realise a rail-to-rail driver. The output buffer has strong driving capability with push–pull function by the current positive feedback (CPF). Therefore the source driver can drive the pixel with two-dot inversion to decrease power consumption. On the other hand, the proposed output buffer with CPF can integrate the offset average to reduce the offset voltage. The performance is experimentally verified with a prototype chip that occupies a silicon area of 1700 × 260 $mm^2$ in a 0.35-mm 2P4M CMOS process. The measured settling time is less than 7.8 ms.

## II. PROPOSED BUFFER AMPLIFIER

The proposed buffer configuration contains biasing network (MB1-MB4), NMOS differential amplifier M5 M6 and M7 for biasing, M8,M17 for folded summing stage and M18,M19 class AB output stage as shown in fig 3. and M8 & M13 current distributed load to increase the active load resistance by decreasing the current flow in MOS M9 & M12.

Input differential amplifier are designed to draw the same current value nIB1/2, whereIB1 is thquiescent current supplied by the partialness network contrivances MB1-MB4 and n is the mirror factor of current sources M1 and M4, defined as

$$n = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_{M1}}$$

Postulating an equal aspect ratio for transistors M8,M9,M12,13 and M11-M17, the currents in both branches of the folded-cascode mirror have the same value. Hence, the drain voltages of M9and M17 are respectively equipollent to those of M15 and M16. The currents flowing in M9 and M11 are given by

$$I_{M11} = I_{M9} = n\frac{I_7}{2} + I_{10}$$

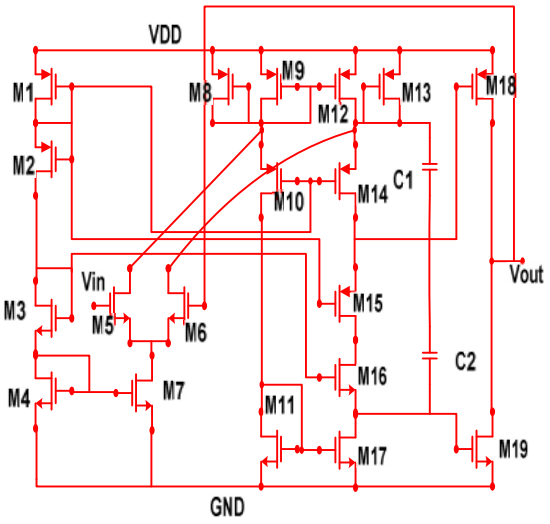


**Fig. 5.**

Since the gate voltages of M10 and M14 are respectively sizing of the current mirror factors of the folded-cascode input stage, and no supplemental biasing networks are required to maintain an virtually constant output current, Consequently, the output quiescent current of the amplifier class-AB section can get opportunely set by betokens of a felicitous W/L ratio of M10 & M14, a push-pull O/P stage M18 &M19, operate in class AB mode will turn ON and OFF according to the current distribution at M9 and M12.

## III. CONCLUSION

It is limpidly visually perceived in the results that the output waveform follows the input waveform. Withal the comparison table depicts a remarkable amelioration of the proposed amplifier over other antecedently reported buffers. Hence the high speed self inequitable low power rail-to-rail class-AB buffer amplifier is implemented prosperously. A comparison table 2 show the different parameters in comparison with previous results. A simulation in micro-wind tool is shown in Fig. 4 with square and triangular wave input.

## IV. FUTURE SCOPE

Since the dissertation topic implements a very compact, high speed rail-to-rail buffer for LCD drivers, it can be utilized as a boon in many future applications where die area is a matter of concern, adscitiously where slew rates is a matter of concern. Since it utilises a only 0.2 mV of static puissance, hence is having tremendous demand in hundreds of exhibit contrivances applications. Due its merits, it can be utilized in following areas-

* Since power consumption is low, it has a great future in getting utilized in applications like “ultra low power ADCs”.
* Since it is utilizing AMLCD technology, the exhibit is amended remarkably, hence can be utilized in “image exhibit contrivances, flat panel exhibits etc.
*Due to rail-to-rail input and output cognations, it is greatly utilized in buffered analog clocks. Above are just few examples, but this buffer is having excellent usability in many other areas supplementally.

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